Ben;

Please see attached my final report from ECE590, and also 3 paper summaries from ECE585.

For 590, I implemented 2 versions of synthesizable VHDL code for median filters for 3x3 kernels in combinatorial logic. Version 1 uses the median of medians algorithm ( <https://en.wikipedia.org/wiki/Median_of_medians> ), version 2 is a true median implementation, and could be expected to consume about double the number of gates (ratio of 7:4), and about 50% bigger gate delay, as 3 stages of comparators are needed instead of 2.

Also, I extended the image processor (VHDL version) to add a median filter for image noise removal. This one relied on the median of medians implementation. I was operating based on the assumption that the Erik Liskay image processor was synthesizable or could be modified. This stole lots of the time available. It is possible that the Liskay project can be changed in some manner to be synthesizable, however, to me this seems like a bigger task than starting from scratch.

I was given 2 prior projects as a starting poing, one was feature rich and not synthesizable (Liskay et. al), the other was synthesizable, but with very limited features, Sumitha et. al. My recommendation would be that the Liskay project only be used for inspiration (it does contain very elegant and beautiful code for creating 100 image processors in parallel), and focus on the Sumitha project.

I think Vivado supports mixed language projects, so you can add my VHDL code if you want to add a median filter to the Sumitha project.

The attached paper summaries are about image processing, I think you might find the Chinese paper outlining howto remove noise followed by detecting edges on images from traffic cams very instructive for your project. That outlines a complete solution which may be useful towards robot vision applications.

Please see link to prior image processing projects on google drive, with 110MB, they are too large for E-mail:

<https://drive.google.com/a/pdx.edu/file/d/0B7FaUDXM8838blVKQUJZOXFrSFU/view?usp=sharing>

Jan Fure

---------- Forwarded message ----------
From: **Jan Fure** <jfure@pdx.edu>
Date: Sat, Nov 1, 2014 at 6:40 PM
Subject: Please see attached ECE590 final report and VHDL code
To: Marek Perkowski <h8mp@pdx.edu>